

Omkar Lonkar

CURRICULUM VITAE

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Research Interests

Computer architecture, hardware design, CPU microarchitecture, ASIC design, reconfigurable and flexible systems; instruction set architecture, ISA extensions; algorithms, graph algorithms, high performance computing; energy efficiency, green computing, sustainable systems.

Teaching Interests

Computer architecture, instruction set architecture, assembly language, logic design.

Education

University of California, Santa Cruz

August 2023 – Present

- Doctor of Philosophy in Computer Science and Engineering
- Master of Science in Computer Science and Engineering

University of California, Santa Barbara

August 2019 – June 2023

- Bachelor of Science, *cum laude*, in Computer Engineering

Professional Appointments

Graduate Student Researcher, University of California, Santa Cruz

August 2023 – Present

- **UCSC Secure Usable Systems Lab and UCSC Sustainable Systems Lab**
 - Architected a processor with on-chip reconfigurability to add hardware support for new floating-point datatypes, improving performance by $3.23\times$, extending hardware lifetime, and cutting manufacturing carbon emissions by $3.41\times$.
 - Built a simulator modeling the total cost of power, energy, and carbon for datacenters from historical workload traces, predicting power distribution unit consumption within 2% of the ground truth to guide datacenter rightsizing.
- **UCSC Vertical Architectures, Memories, and Algorithms Group**
 - Designed a novel distributed-memory graph triangle counting algorithm using Bloom filters for vertex neighbor list compression, reducing inter-processing-element message count by $10.61\times$ and improving algorithm runtime by $8.46\times$ [U1].

Teaching Assistant, University of California, Santa Cruz

March 2024 – Present

- Assisting in teaching of undergraduate-level courses in the Department of Computer Science and Engineering.

Science Internship Program Mentor, University of California, Santa Cruz

June 2026 – Present

- Mentoring high school students in conducting research in computer architecture.
- Developing an instruction set architecture and processor implementation to be used in computer architecture courses at UC Santa Cruz.

Software Engineering Intern, Siemens EDA

June 2022 – September 2022

- Developed runtime systems for the Veloce Prototyping System (VPS), enabling the open-source manycore processor OpenPiton to run on VPS.
- Synthesized a 64-core OpenPiton design with an 8×8 array of Ariane tiles onto a Xilinx VU19P FPGA, validating the runtime by booting Linux at scale.

Undergraduate Research Experience

UCSB ArchLab

June 2021 – June 2023

- Benchmarked Cohort, a system that exploits the behavior of shared-memory queues to efficiently connect producers and consumers in software with hardware accelerators, achieving speedups of up to $8.38 \times$ over MMIO and $11.24 \times$ over DMA, improving performance by $2.32 \times - 8.10 \times$.
 - Published in ASPLOS '23.
- Developed a research tool to allow users to create and compare hardware implementations of branch predictors.

Fellowships

2023–2024 University of California Regents Fellowship

2023–2024 Computer Science and Engineering Department Fellowship, UC Santa Cruz

Honors and Awards

2023 *Cum Laude*, University of California, Santa Barbara

2021 Tau Beta Pi Honor Society Inductee, University of California, Santa Barbara Chapter

2020–2023 College of Engineering Honors Program, University of California, Santa Barbara

2019–2023 Dean's List, University of California, Santa Barbara

Teaching

Courses Assisted

CSE 120: Computer Architecture, UC Santa Cruz

Sp'24, Wi'25, Wi'26, Sp'26

- Developing PyRTL-based labs for upper division Bachelors-level Computer Architecture course.
- Taught discussion sections; assisted in creating exams, assignments and practice problem sets; and graded coursework.

- Assisted in creating Jupyter-based assignments, taught discussion sections, and graded exams.

Students Supervised & Mentored

Legend: ▽ bachelor's/master's research; ★ UCSC SIP.

Past Mentees

Name	Years	Degree, Institution	Employer/Next Step
Bronsen Lasala ▽ [P1]	2026– 2026	B.S., UC Santa Cruz	
Jeanelle Dao ★	2026– 2026	Presentation High School	
Orion Ghai ★	2026– 2026	Los Gatos High School	
Harshita Vohra ★	2026– 2026	Irvington High School	

Scholarly and Creative Work

Conference Publications (Peer Reviewed)

[C1] Tianrui Wei, Nazerke Turtayeva, Marcelo Orenes-Vera, Omkar Lonkar, and Jonathan Balkind. 2023. Cohort: Software-Oriented Acceleration for Heterogeneous SoCs. In Proceedings of the 28th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 3 (ASPLOS 2023). Association for Computing Machinery, New York, NY, USA, 105–117. <https://doi.org/10.1145/3582016.3582059>

Preprints, Manuscripts in Preparation

[U1] O. Lonkar, and S. Beamer. “Accelerating Distributed Memory Triangle Counting Using Bloom Filters.”

Theses

[R1] O. Lonkar. “Accelerating Distributed Memory Triangle Counting Using Bloom Filters,” *M.S. Thesis*, UC Santa Cruz, 2025.

Conference, Workshop, and Center Presentations

[P1] Modeling Power Usage in Data Centers. Center for Research in Systems and Storage IAB Meeting, 2026.